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REMARKS

In response to the Office Action dated January 9, 2007, no claims are amended, no claims are cancelled, and no claims are added. Claims 1-13 are now active in this application. No new matter has been added.

Claims 1 and 3 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kimura et al. (U.S. 5,210,479) in view of Takanashi et al (U.S. 6,351,399) and further in view of Kohno et al. (U.S. 6,180,966).

Claims 2 and 4 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kimura in view of Takanashi and Kohno and Marquardt (U.S. 5,650,906) and Official Notice of operational amplifiers.

Claims 5-8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kimura in view of Takanashi and Kohno and Horowitz.

Claims 9 and 10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kimura in view of Takanashi and Kohno and case law (*In re Larson*, 340 F. 2d 965, 968, 144 USPQ 247, 349 (CCPA 1965)).

Claims 11-13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wacknov et al. (U.S. 6,812,586) in view of Kimura and Takanashi and Kohno.

These rejections are traversed. and the Official Notice is traversed.

Independent claim 1 recites, in pertinent part, "a **first comparator which detects a collector voltage of said power semiconductor device to output a first detection signal when the detected collector voltage exceeds a first reference voltage.**"

In one example of claim 1, as illustrated in FIG. 1 of the application, the gate voltage is compared with the first reference voltage and the collector voltage is compared with the second

reference voltage at the first and second comparators, respectively. When both of the gate and collector voltages exceed the first and second reference voltages, respectively, the protection signal is generated. Since two different comparators and two different reference voltages are provided, the protection of the semiconductor device can be securely made without a false detection of short circuit state.

Similarly, independent claim 11 recites, in pertinent part, "a first comparator which detects a collector voltage of said power semiconductor device to output a first detection signal when the detected collector voltage exceeds a first reference voltage."

In order to establish a *prima facie* obviousness under 35 U.S.C. § 103(a), all the claim limitations must be taught or suggested by the prior art. *In re Rokya*, 490 F. 2d 981, 180 USPQ 580 (CCPA 1974). Further, "rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *In re Kahn*, 441 F. 3d 977, 988 (Fed. Cir. 2006). At a minimum, the cited prior art does not disclose (expressly or inherently) the above recited limitations of Applicant's respective independent claims.

The Office Action, at page 2, asserts that Kimura, at FIG. 8, elements 12, 13, 15, 23, 3, and 5, satisfies the first comparator requirements of claim 1.

Kimura, at column 9, line 45 to column 10, line 6, merely states:

> FIG. 8 is a circuit diagram showing the fourth preferred embodiment of the present invention. It is different from the first embodiment in FIG. 1 in that a second overcurrent detecting circuit comprises a PNP transistor 31 having a base connected to the condenser 19 through a resistor 32, and a resistor 33 and a diode 34. A collector-emitter current path of the PNP transistor 31, the resistor 33 and the diode 34 are connected in series between the gate of IGBT 10 and the connection node A. And the condenser 13 is connected to the connection node A and the power supply 2 for the substantially same function as one in the first embodiment in FIG. 1.

> In other words, the gate voltage Vg of IGBT 10 is supplied to the emitter of the PNP transistor 31 through the diode 34 having a forward drop voltage V_{DF} and the voltage of the capacitor 19 as the predetermined reference value Vgs is supplied to the base of the PNP transistor 31 through the resistor 32. In the case of $Vg- V_{DF} > Vgs$, $(Vg > Vgs+V_{DF})$, the PNP transistor 31 turns into the ON state, the voltage $(Vg31\ V_{DF})$, which is based on the gate voltage Vg, is output as a second overcurrent detection signal through the resistor 33. This output node is connected to the connection node A of the first overcurrent detecting circuit comprising the resistor 11 and the diode 12. In this way, the connection point A outputs a logical AND of the first and second overcurrent detection signals.
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> The operations of the second overcurrent detecting circuit in the fourth embodiment in FIG. 8 are explained by the timing chart in FIG. 9.

Additionally, see Kimura's FIG. 1, and column 3, line 40 to column 7, line 31 for additional discussion of some of the elements of FIG. 8, although in a different configuration.

It is respectfully submitted that Kimura's elements 12, 13, 15, 23, 3, and 5 in Fig. 8, merely form an "ON holding circuit" when the overcurrent detection circuit comes into operation so as to hold the ON-state in a delay period until the gate voltage becomes down to some degree. This ON-hold operation period is determined by the time constant of capacitor 21 and resistor 24 connected to the transistor 23.

The cited elements of Kimura do not work as "a first comparator which detects a collector voltage of said power semiconductor device to output a first detection signal when the detected collector voltage exceeds a first reference voltage," as required by claim 1.

Additionally, Takahashi and Kohno do not remedy the deficiencies of Kimura. For example, Takahashi, at Abstract, is merely directed to "supplying electric power to the level shift circuit and a negative pole of the switching semiconductor element are connected to each other through at least one of an inductor and a resistor." Kohno, at FIGs. 1 and 2, merely discloses a trench IGBT.

Thus, Applicant submits that independent claim 1 is patentable over the combination of Kimura, Takahashi, and Kohno.

Further, Marquardt, Official Notice of operational amplifiers, Horowitz, *In re Larson*, 340 F. 2d 965, 968, 144 USPQ 247, 349 (CCPA 1965), and Wacknov do not remedy the deficiencies of Kimura. For example, Marquardt, at Abstract, merely discloses a "comparator which has a downstream analog amplifier with a limiting characteristic curve," at Abstract and at column 2 lines 58-67. The Official Notice merely states, at Office Action, page 5, that "some operational amplifiers (and comparators as well) allow only a limited voltage between inputs." *In re Larson* merely supports the proposition that "one piece construction . . . would be merely a matter of obvious engineering design choice." Wacknov, at Abstract, merely discloses "an AC/DC power converter."

Thus, Applicant submits that independent claim 11 is patentable for reasons similar to independent claim 1.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as independent claims 1 and 11 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable.

Thus, it is respectfully submitted that dependent claims 2-10, 12, and 13 are also patentable for at least the same reasons as their respective base claims.

Accordingly, it is urged that the application, as now amended, is in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, Examiner is requested to call Applicant's attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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